

# (12) UK Patent Application (19) GB (11) 2 265 049 (13) A

(43) Date of A publication 15.09.1993

(21) Application No 9217754.2

(22) Date of filing 20.08.1992

(30) Priority data

(31) 0483345

(32) 03.03.1992

(33) JP

(71) Applicant

Mitsubishi Denki Kabushiki Kaisha

(Incorporated in Japan)

No. 2-3 Marunouchi 2-chome, Chiyoda-ku, Tokyo 100,  
Japan

(72) Inventor

Yasuaki Yoshida

(74) Agent and/or Address for Service

Marks & Clerk

57-60 Lincoln's Inn Fields, London, WC2A 3LS,  
United Kingdom

(51) INT CL<sup>5</sup>

H01L 21/385

(52) UK CL (Edition L)

H1K KLBB K1EB K2R3E K2S12 K2S23 K2S27  
K2S5 K3E1M K3E5CY K3F K8VE K9E K9N2 K9N3  
K9R2

(56) Documents cited

None

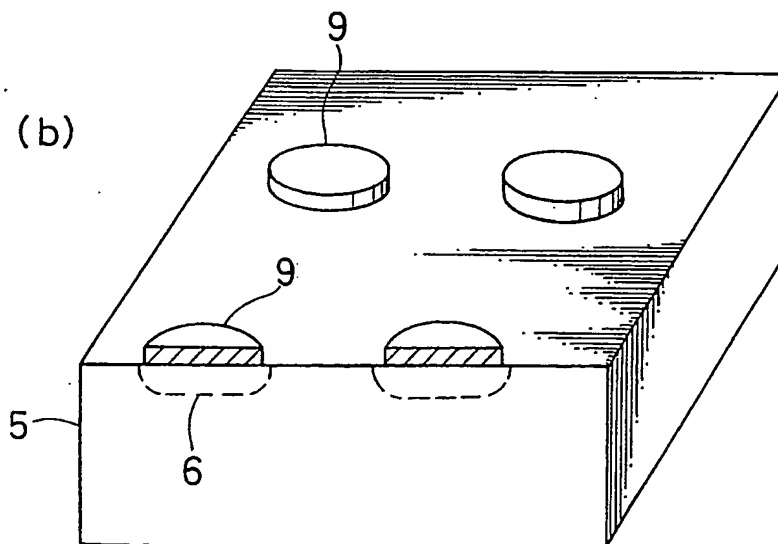
(58) Field of search

UK CL (Edition K) H1K KLBA KLBB KLBC KLBE  
KLBX  
INT CL<sup>5</sup> H01L

(54) A method for producing a II-VI semiconductor device

(57) In a method for producing a II-VI compound semiconductor device including mercury, a thin film 9 comprising a group II element or a group II compound, which is solid at a room temperature, is deposited on a surface of a p type II-VI compound semiconductor 5, and annealing is carried out to diffuse the group II element from the thin film into the p type II-VI compound semiconductor, whereby a region of the p type II-VI compound semiconductor, on which the thin film is present, is converted to n type, resulting in a p-n junction 6. Therefore, instruments and material are easily handled, increasing work efficiency and productivity. In addition, the annealing is carried out without a complicated temperature profile, resulting in a simple process.

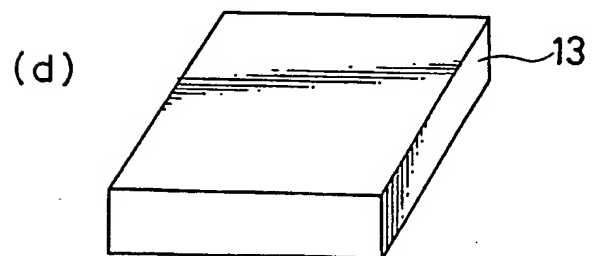
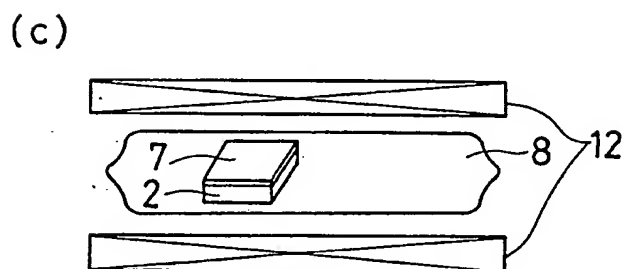
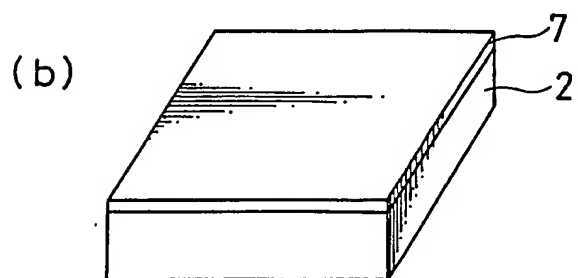
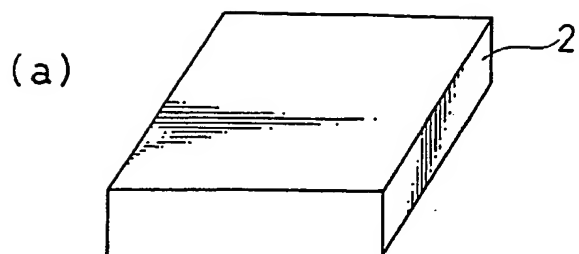
FIG. 2 (b)



GB 2 265 049 A

1/6

FIG. 1



2/6  
FIG. 2

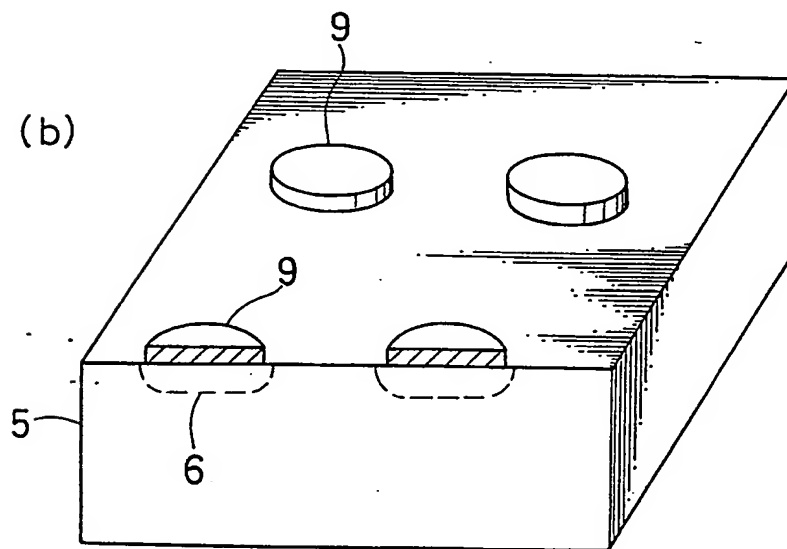
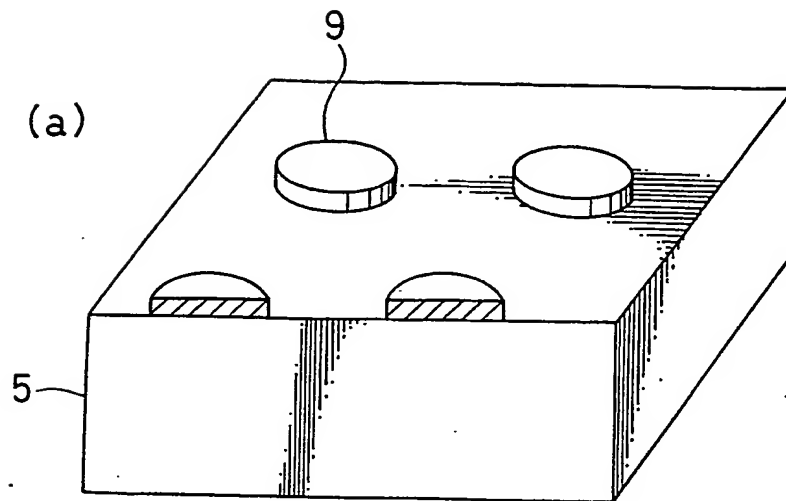
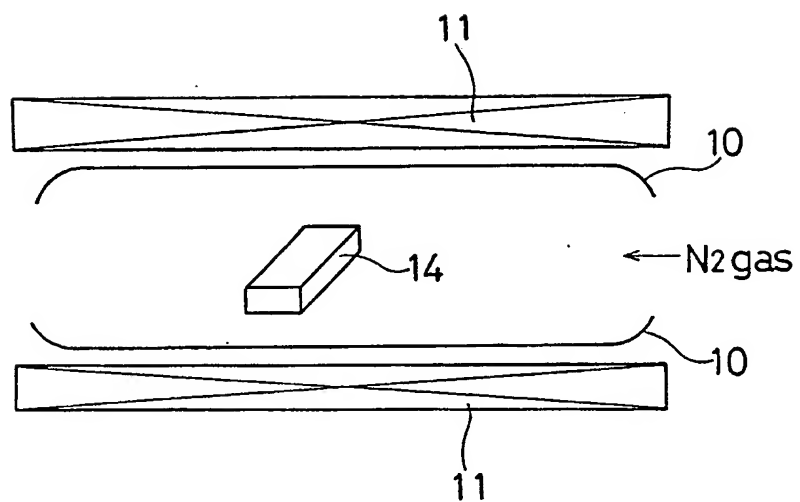


FIG. 3



A/G

FIG. 4 (PRIOR ART)

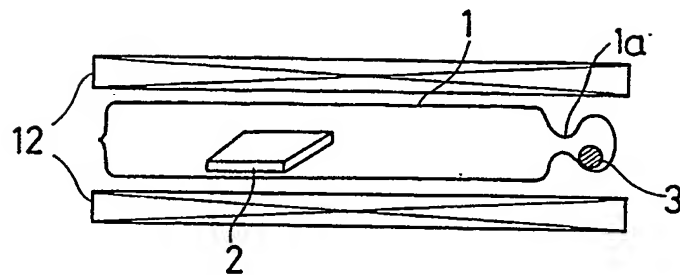
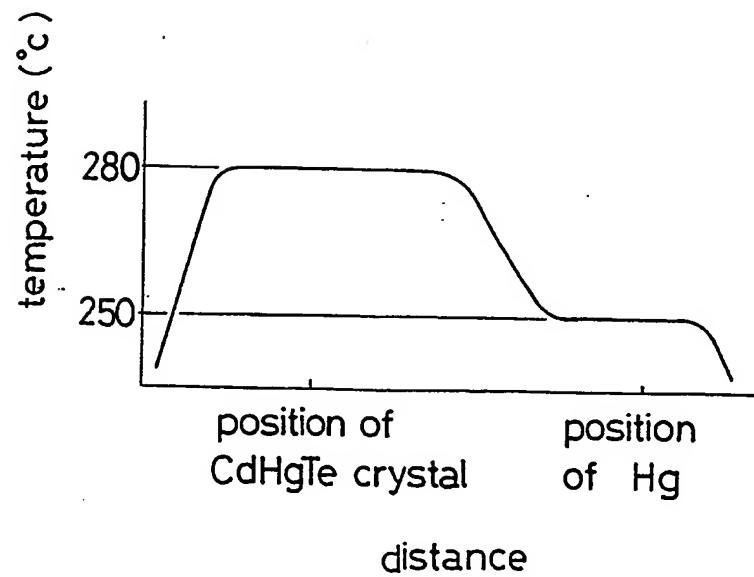
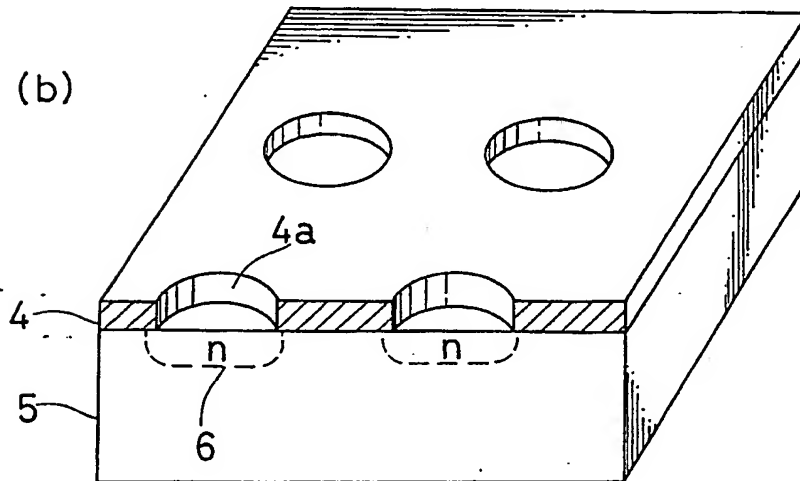
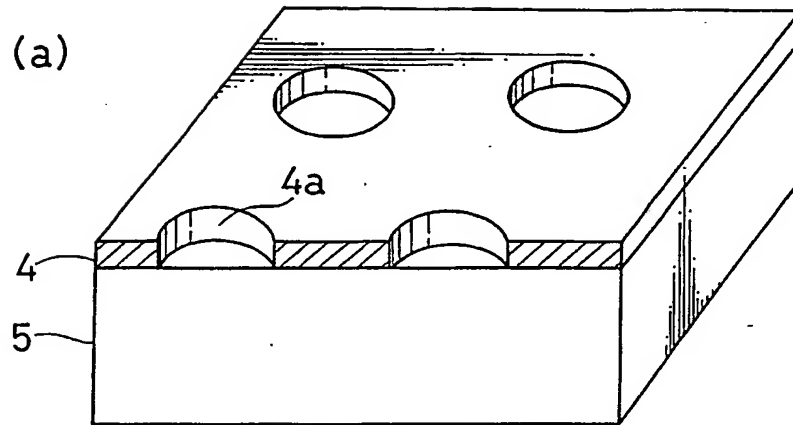


FIG. 5 (PRIOR ART)



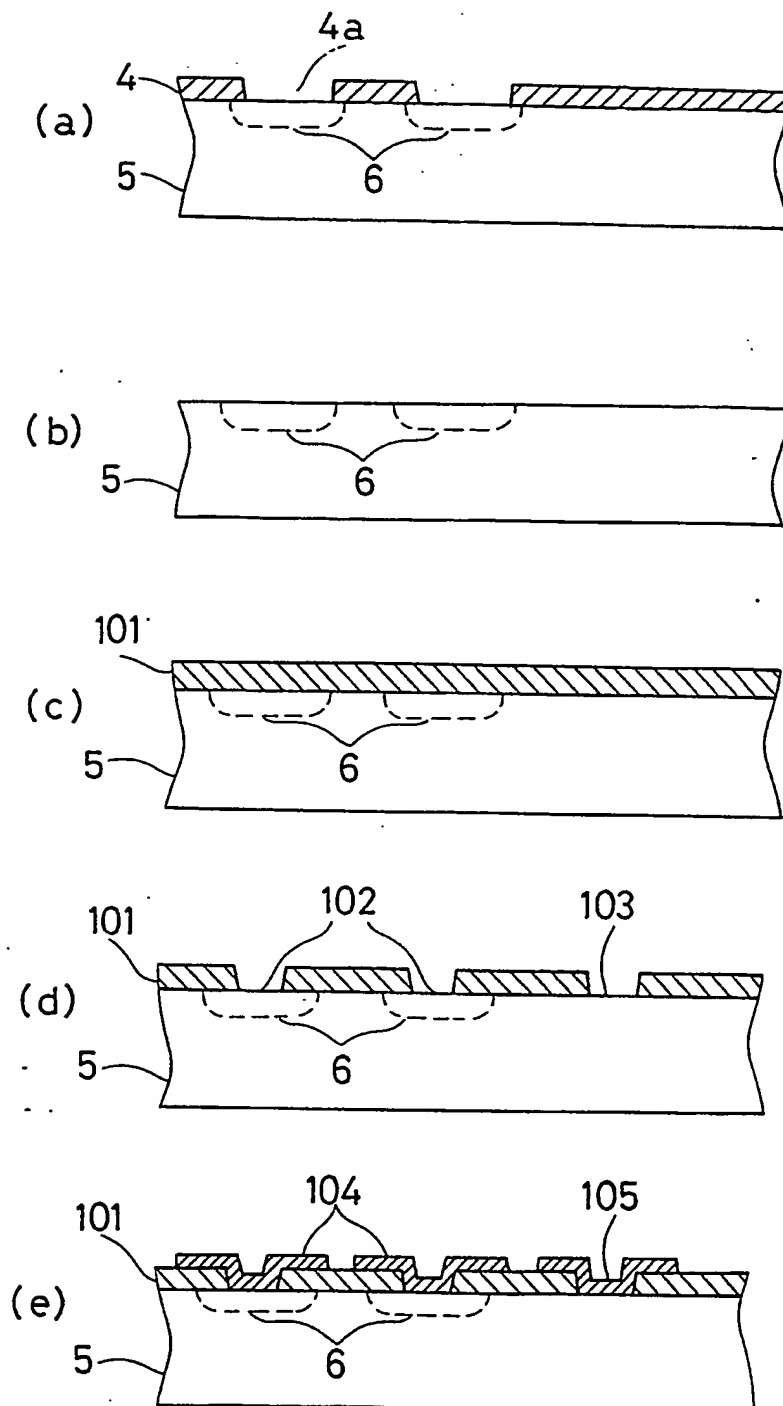
5/6

FIG. 6 (PRIOR ART)



6/6

FIG. 7 (PRIOR ART)



## A METHOD FOR PRODUCING A SEMICONDUCTOR DEVICE

The present invention relates to a method for producing a semiconductor device and, more particularly, to a method for controlling a conductivity type of a II-VI semiconductor including mercury which is used as a material of an infrared detector.

A compound semiconductor comprising a II-VI mixed crystal, such as a CdHgTe crystal, has a property that energy band gap thereof is changed by changing composition ratio of the crystal, so that it is used as a material of a low-noise photodetector or the like.

Figure 4 is a schematic diagram for explaining a process for controlling a conductivity type in a method for producing a II-VI compound semiconductor device, disclosed in Japanese Patent Publication 62-34157. In figure 4, a CdHgTe crystal 2 is enclosed in a quartz ampoule 1 with mercury 3 which is liquid state at a room temperature. The mercury 3 is separated from the CdHgTe crystal 2 by the narrow part 1a of the ampoule 1, i.e., a mercury reservoir is provided at an end of the ampoule 1. Heaters 12 are disposed in the neighborhood of the ampoule 1.

Since mercury (Hg) has a very high vapor pressure, Hg is dissociated from the CdHgTe crystal 2 during the crystal



growth, resulting in vacancies in the CdHgTe crystal. The vacancies serve as acceptors. For example, a CdHgTe crystal grown by liquid phase epitaxy (LPE) includes a lot of Hg vacancies and has a p type carrier concentration as high as  $\sim 10^{17} \text{cm}^{-3}$ , so that the mobility of carrier is low.

Therefore, it is impossible to use the CdHgTe crystal for a semiconductor device. In order to solve this problem, as shown in figure 4, the CdHgTe crystal 2 is loaded in the ampoule 1 with mercury 3, the ampoule is evacuated to  $10^{-6}$  Torr, and an annealing is carried out at an appropriate temperature using the heaters 12. During the annealing, Hg partial pressure from the mercury 3, which is produced in the ampoule, is applied to the CdHgTe crystal 2 to fill up the vacancies in the crystal, whereby the CdHgTe crystal having such a high carrier concentration is converted to a p type CdHgTe crystal having a low carrier concentration. If the Hg partial pressure is applied to the crystal until most of the vacancies are filled up, an n type CdHgTe crystal is obtained.

The annealing process for reducing carrier concentration of the CdHgTe crystal will be described in more detail using a temperature profile of figure 5. The CdHgTe crystal 2 in the ampoule 1 is heated up to  $280^\circ \text{C}$  while the mercury 3 is heated up to  $250^\circ \text{C}$ , whereby Hg partial pressure is applied to the CdHgTe crystal 2. The

CdHgTe crystal 2 and the mercury 3 are kept in this state for about twenty four hours to diffuse Hg into the CdHgTe crystal 2 without Hg being applied to the inner wall of the ampoule 1, resulting in an n type CdHgTe crystal having a carrier concentration of approximately  $10^{14}\text{cm}^{-3}$ .

Figures 6(a) and 6(b) are schematic diagrams for explaining a method for producing p-n junctions in a II-VI compound semiconductor including mercury by a diffusion of mercury. A diffusion mask 4 comprising Zn and having a thickness of about 1 micron is disposed on a p type CdHgTe crystal 5 about 10 microns thick. A plurality of apertures 4a each having a diameter of about 1 to 30 microns are formed through the diffusion mask 4.

The CdHgTe crystal 5 with the diffusion mask 4 is loaded in a quartz ampoule with mercury as shown in figure 4 and annealed. During the annealing, prescribed Hg partial pressure is applied to the surface of the CdHgTe crystal 5 exposed in the apertures 4a of the diffusion mask 4, whereby n type regions are formed as shown in figure 6(b), resulting in p-n junctions 6 at depth of about 3 microns.

Figures 7(a)-7(e) are cross-sectional views of steps in a method for producing, for example, a photodiode array using the p-n junctions 6. After the p-n junctions 6 are formed in the CdHgTe crystal 5 as shown in figure 7(a), the diffusion mask 4 is removed as shown in figure 7(b). Then,

an oxide film 101 is deposited on the entire surface of the CdHgTe crystal 5 as shown in figure 7(c). Subsequently, n side contact holes 102 are formed on the n type regions and a p side contact hole 103 is formed on the CdHgTe crystal 5 using a conventional photolithography as shown in figure 7(d). Then, a metal layer is deposited on the wafer and patterned as shown in figure 7(e), resulting in n side electrodes 104 connecting to the CdHgTe crystal 5 through the contact holes 102 and 103 and a p side electrode 105 connecting to the CdHgTe crystal 5 through the contact hole 103.

In Japanese Patent Published Application No. 58-171848, a small quantity of group III element, such as indium, is added as a donor impurity during the growth of a CdHgTe crystal and then annealing is carried out to control the quantity of Hg in the CdHgTe crystal, whereby carrier concentration is controlled. Meanwhile, in Japanese Patent Published Application No. 62-13085, a bump electrode comprising indium is formed on a CdHgTe layer and then annealing is carried out to convert a region of the CdHgTe layer, on which the bump electrode is present, to n type. In these conventional methods, however, the indium as a donor impurity becomes a scattering factor in the crystal, so that the mobility of carrier is not improved so much, resulting in a semiconductor device with poor electrical

characteristics.

In the above-described methods for producing semiconductor devices, the mercury, which is liquid at a room temperature, is used as means for applying Hg vapor pressure to the II-VI crystal including mercury atom. Therefore, if the ampoule is inclined, the mercury moves and it is difficult to obtain a desired temperature profile. Therefore, the ampoule should be treated with the greatest possible care, so that the work efficiency is unfavorably reduced.

In addition, as shown in the temperature profile of figure 5, the annealing should be carried out with the CdHgTe crystal 2 kept 30°C warmer than the Hg reservoir, to avoid Hg from adhering to the inner wall of the ampoule, and this results in a complicated process. In addition, when the group III element is used as a donor impurity, it acts as a scattering factor and the mobility of carrier is not improved.

#### SUMMARY OF THE INVENTION

It is an object of the present invention to provide a method for producing a semiconductor device, in which instruments and materials are easily handled with high work efficiency and a control of conductivity type of a II-VI semiconductor crystal including mercury and a production of p-n junction in the II-VI semiconductor crystal are

performed in a simple process without using a donor impurity.

Other objects and advantages of the present invention will become apparent from the detailed description given hereinafter; it should be understood, however, that the detailed description and specific embodiment are given by way of illustration only, since various changes and modifications within the spirit and scope of the invention will become apparent to those skilled in the art from this detailed description.

According to a first aspect of the present invention, a group II element is diffused into a II-VI crystal including mercury, using a group II element or a group II compound, which is solid at a room temperature, as a diffusion source, to control the conductivity type of the crystal. Therefore, instruments and materials are easily handled and an annealing for the diffusion is carried out with a uniform temperature profile.

According to a second aspect of the present invention, a thin film comprising a group II element or a group II compound, which is solid at a room temperature, is formed on a surface of a p type II-VI compound semiconductor and then annealing is carried out to diffuse the group II element into a region of the p type II-VI compound semiconductor, on which the thin film is present, to convert the region into n

type, whereby a p-n junction is formed. Therefore, instruments and materials are easily handled, and the annealing is carried out with a uniform temperature profile.

#### BRIEF DESCRIPTION OF THE DRAWINGS

Figures 1(a)-1(d) are diagrams of steps in a method for controlling a conductivity type of a CdHgTe crystal in accordance with a first embodiment of the present invention;

Figures 2(a) and 2(b) are diagrams of steps in a method for producing p-n junctions in a CdHgTe crystal in accordance with a second embodiment of the present invention;

Figure 3 is a schematic diagram for explaining an annealing process using an open-tube type annealing furnace in accordance with the first and second embodiments of the present invention;

Figure 4 is a schematic diagram for explaining a method for controlling a conductivity type of a CdHgTe crystal in accordance with the prior art;

Figure 5 is a diagram showing a temperature profile used in the method shown in figure 4;

Figures 6(a) and 6(b) are diagrams of steps in a method for producing p-n junctions in a p type CdHgTe crystal in accordance with the prior art; and

Figures 7(a)-7(e) are sectional views of steps in a method for producing a photodiode array in accordance with

the prior art.

#### DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Figures 1(a)-1(d) are schematic diagrams illustrating steps in a method for producing a semiconductor device in accordance with a first embodiment of the present invention. In figure 1, the same reference numerals as in figure 4 designate the same or corresponding parts. A Zn thin film 7 about 1000 angstroms thick is disposed on a surface of a CdHgTe crystal 2 about 10 microns thick.

First of all, a CdHgTe crystal 2 shown in figure 1(a) is prepared. Then, a Zn thin film 7 about 1000 angstroms thick is deposited on the surface of the CdHgTe crystal 2 by sputtering or the like as shown in figure 1(b). Then, as shown in figure 1(c), this wafer is loaded in an ampoule 8 and the ampoule 8 is evacuated to  $10^{-6}$  Torr. Then, the wafer is annealed at 200 °C for twenty hours using the heater 12. During the annealing, Zn particles are diffused into the CdHgTe crystal and fill up Hg vacancies in the CdHgTe crystal 2. After the annealing, the wafer is taken out of the ampoule 8 and the Zn thin film is removed by etching, providing an n type CdHgTe crystal 13 having a carrier concentration of about  $10^{14} \text{ cm}^{-3}$  as shown in figure 1(d).

According to the first embodiment of the present invention, Zn, which is solid at a room temperature, is used for filling up the acceptors in the CdHgTe crystal 2. More

specifically, the Zn thin film 7 is deposited on the CdHgTe crystal 2 and annealed to diffuse the Zn particles into the CdHgTe crystal 2. Therefore, the materials are easily treated, increasing the work efficiency. In addition, since the annealing is carried out with a uniform temperature profile, the process is simplified. In addition, since Zn is a group II element like Cd and Hg, it fills up an acceptor and combines with a group VI element, so that Zn does not act as a scattering factor, with the result that the carrier mobility is significantly improved.

Figures 2(a) and 2(b) are schematic diagrams illustrating steps in a method for producing p-n junctions of a photodiode array in accordance with a second embodiment of the present invention.

First of all, as shown in figure 2(a), a plurality of Zn thin films each having a thickness of about 1000 angstroms and a diameter of about 1 to 30 microns are formed on a surface of a p type CdHgTe crystal 5 about 10 microns thick by transcribing technique. Then, this wafer is loaded in the ampoule in the same manner as described in the first embodiment and annealed at 200 °C for about ten hours. During the annealing, Zn particles are diffused into regions in the CdHgTe crystal 5 where the Zn films are present, resulting in n type regions having a carrier concentration of about  $10^{14}\text{cm}^{-3}$ . Thus, p-n junctions 6 are formed at



depth of about 3 microns in the CdHgTe crystal 5, as shown in figure 2(b).

In the above-described embodiments, although the CdHgTe crystal 2 (5) with the Zn thin film is set in the ampoule under vacuum and annealed, an open-tube type annealing furnace shown in figure 3 may be used because Zn is solid at a room temperature and there is no necessity of regarding vapor pressure, differently from Hg. In figure 3, reference numeral 10 designates a quartz tube and reference numeral 14 designates a CdHgTe crystal on which a Zn thin film is formed.

During the annealing, nitrogen gas or the like is introduced into the quartz tube 10 while heating the quartz tube at a desired temperature by the heater 11, whereby Zn particles are diffused into the CdHgTe crystal. Since the open tube 10 is used instead of an ampoule, the step of evacuating the ampoule is dispensed with. Therefore, this method is suited for a large-sized wafer. In this case, however, reproducibility of the process is reduced a little.

While in the above-described embodiments Zn is used as a group II element, other group II elements or group II compounds may be used with the same effects as described above.

While in the above-described embodiments the CdHgTe crystal is used as a II-VI compound semiconductor including

Hg, other II-VI compound semiconductor including Hg may be used.

As is evident from the foregoing description, according to the present invention, a group II element, such as Zn, is diffused into a group II-VI crystal including Hg; using a group II element or a group II compound, which is solid at a room temperature, as a diffusion source, whereby conductivity type of the group II-VI crystal including Hg is controlled, or p-n junctions are formed in the group II-VI crystal including Hg. Therefore, instruments and materials are easily handled, increasing work efficiency and productivity. In addition, an annealing for the diffusion is carried out without using a complicated temperature profile, resulting in a simple process.

WHAT IS CLAIMED IS:

1. A method for producing a II-VI compound semiconductor device including mercury, comprising:

producing a II-VI crystal using a group II element, a group VI element, and mercury; and

diffusing a group II element into said II-VI crystal using as a diffusion source a group II element or a group II compound, which is solid at a room temperature, to control conductivity type of said II-VI crystal.

2. A method for producing a semiconductor device including a step of controlling conductivity type of a p type II-VI compound semiconductor including mercury, comprising:

depositing a thin film comprising a group II element or a group II compound, which is solid at a room temperature, on a surface of said p type II-VI compound semiconductor; and

performing an annealing to diffuse said group II element from said thin film into said p type II-VI compound semiconductor, whereby a region of said p type II-VI compound semiconductor, on which said thin film is present, is converted to n type, resulting in a p-n junction.

3. The method of claim 1 wherein said solid-phase

diffusion is carried out under atmospheric pressure.

4. The method of claim 2 wherein said solid-phase diffusion is carried out under atmospheric pressure.

5. The method of claim 1 wherein said group II element is zinc and said group II compound is zinc compound.

6. The method of claim 2 wherein said group II element is zinc and said group II compound is zinc compound.

7. A method of producing a semiconductor device, substantially as herein described with reference to figures 1 to 5 of the accompanying drawings.

14

**Patents Act 1977**  
**Examiner's report to the Comptroller under**  
**Section 17 (The Search Report)**

Application number

GB 9217754.2

**Relevant Technical fields**

(i) UK CI (Edition K ) H1K (KLBA, KLBB, KLBC, KLBE, KLBX)

(ii) Int CI (Edition 5 ) H01L

**Databases (see over)**

(i) UK Patent Office

(ii)

**Search Examiner**

W A MORRIS

**Date of Search**

22 SEPTEMBER 1992

Documents considered relevant following a search in respect of claims ALL

Category (see over)	Identity of document and relevant passages	Relevant to claim(s)
	NONE	

Category	Identity of document and relevant passages	Relevant to claim(s)

#### Categories of documents

X: Document indicating lack of novelty or of inventive step.

Y: Document indicating lack of inventive step if combined with one or more other documents of the same category.

A: Document indicating technological background and/or state of the art.

P: Document published on or after the declared priority date but before the filing date of the present application.

E: Patent document published on or after, but with priority date earlier than, the filing date of the present application.

&: Member of the same patent family, corresponding document.

**Databases:** The UK Patent Office database comprises classified collections of GB, EP, WO and US patent specifications as outlined periodically in the Official Journal (Patents). The on-line databases considered for search are also listed periodically in the Official Journal (Patents).